Curriculum vitae

Personal information

Surname(s) / First name(s)	Mayakar Praveen
Address(es)	Tunavägen, 39B:1403, 22363, Lund, Sweden
Mobile(s)	+46722002280
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Nationality(-ies)	Indian
Date of birth(DD-MM-YY)	08-01-81
Swedish Personal Number	810108-2538
Gender	Male

Desired employment / Occupational field

Embedded Systems/ ASIC/FPGA Design

Work experience

Dates	Dec 2005 - May 2007
Occupation or position held	Embedded software engineer
Main activities and responsibilities	Development and maintenance of Custom made RTOS using VxWorks Kernel, Project documentation and support. Trained 5 new employees to upgrade their skills to tune work environment.
Name and address of employer	Orion Software services for Bombardier India Ltd, Baroda, India
Type of business or sector	Automobiles/Transportation
Dates	Apr 2005 to Dec 2005
Occupation or position held	Software Engineer
Main activities and responsibilities	Developing and maintenance of products for continuous production services, Maintenance and support for products to be provided to the clients
Name and address of employer	Sovereign Technologies, Bangalore
Type of business or sector	Information Technology & Services
Dates	Aug 2003 to Apr 2005
Occupation or position held	Software Engineer
Main activities and responsibilities	Development and maintenance of web based software, Application Support to facilitate continuous production services, Maintenance and support for products to be provided to the clients
Name and address of employer	24/7 Customer Services, Bangalore, India
Type of business or sector	Information Technology Enabled Services

Education and training

Dates	Aug 2007 till date
Title of qualification awarded	Master in System on Chip (On-going)
Principal subjects/Occupational skills covered	IC Design (ASIC/FPGA), DSP Design
Name and type of organisation providing education and training	Lunds tekniska högskola

Academic Project Work

Project Title	Effective Implementation of hardware accelerated realtime kernel on FPGA (ongoing)
Description	The requirement is to prepare a state of the art for the Real time kernel Sierra. Implement and investigate new methods of using device drivers and effective data structures to facilitate easy implementation of a application using the Sierra APIs. Investigate optimizations in hardware acceleration. The project is being done for AGSTU AB, Vasteras.
Project Title	Mixed Radix FFT (ongoing)
Description	The requirement is to implement using an effective architecture mixed radix FFT/IFFTs on hardware. FFT2, FFT3 & FFT5 are expected to be implemented. Currently A Radix 2 FFT implementation with SDF architecture is done and being validated. The project is a requirement of a larger project used for Channel estimation for LTE standards
Project Title	Implementation of matrix multiplier for 130nm ASIC
Description	A (4x3) input matrix was multiplied with a coefficient matrix of order (3x4). The coefficient values were read from ROM and the product matrix was written on a RAM. The design was optimized for speed and the implementation used 17 clock cycles and operated at 188Mbps. The approach towards the project was very modular and structured
Project Title	Implementation of Block floating point scaling using Cellular neural networks
Description	This project aimed at building a cellular neural network node which operates with a data path of 8 bits (21 bits in ALU). The computational aspects of the data path are then trimmed to fit the BRAM blocks of 8 bit wide. Further the project aims at building a network of such nodes which would communicate the data processed within each. A template function which has tanh functionality processed by the ALU and trimmed into the memory
Project Title	Cepstrum analysis of vocal signal
Description	The project's objective was to develop a program which estimates the pitch of a person singing into a microphone. The audio samples were processed using the concept of cepstrum-analysis to extract the fundamental frequency from the harmonics. With an initial concept of having to estimate the pitch of a singer and compare it with that of the original singer's pitch. In the end an implementation of cepstrum analysis as a pitch estimation algorithm was created.
Project Title	Implementation of Network Attached Storage system on Spartan board
Description	The objective of the project was to implement a network attached storage system where in a flash based storage will be accessible from the UART as well as through the network, via FTP. A Spartan 3 Board was used with the on board LCD display to make a menu based accessible system. We had two subsystems independently working viz., running linux version on the board and a LCD controller and driver with PS2 controller
Project Title	Implementation of cursor movement on a screen through a FPGA
Description	The objective of the project was to implement cursor motion by controlling the input signals of an onboard VGA controller controlled through a FPGA. The project involved building schematics, state machines and coding in VHDL to achieve the functionalities to move the cursor using the arrow keys of the keyboard connected through serial interface. The VGA monitor had to be filled with a background color and a multi-colored cursor (both controlled and generated by the state machines) and when the cursor was moved the background color had to be retained

Personal skills and competences

Language(s)
Self-assessment

	Understanding		Speaking		Writing
	Listening	Reading	Spoken interaction	Spoken production	
English	Fluent	Fluent	Fluent	Fluent	Fluent
Hindi	Fluent	Fluent	Fluent	Fluent	Fluent
Swedish	Beginner	Beginner	Beginner	Beginner	Beginner

Social skills and competences

Good communication skills, able to handle tense situations and deliver and can build good rapport with people.

Organisational skills and competences

Willingness to learn , Team Facilitator with trait as leadership & Good verbal, written and presentation skills

Technical Skills

Core Programming Skills

C & VHDL

Operating Systems

Windows, Linux & VxWorks.

Toolset

Xilinx (ISE &EDK), Altera, Tornado IDE, Synopsys Design vision, SoC encounter & Cadence, Code composer studio.

Artistic skills and competences

Photography and writing.

References

Prof. Lambert Spaanenburg
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